In the Claims:

No amendments to the claims are presented.

1. (Previously presented) An integrated protection circuit for an integrated circuit device, comprising:

a first transistor whose control outputs are connected between a pad and a control input of a clamping device,

control outputs of said clamping device being connected between said pad and a reference voltage terminal,

a second transistor whose control outputs are connected between the control input of the clamping device and said reference voltage terminal, and

time-delay means connected between a supply voltage terminal and control inputs of said first transistor and said second transistor.

2. (Previously presented) The protection circuit according to claim 1, wherein the pad is a signal pad or a power supply pad.

3. (Previously presented) The protection circuit according to claim l, wherein the time-delay means comprises a series connection of a resistor and a capacitance.

4. (Previously presented) The protection circuit according to claim 3, wherein the time-delay means comprises a third transistor, the resistor being connected between the supply voltage terminal and said third transistor, said third transistor forming the capacitance.

5. (Previously presented) The protection circuit according to claim 4, wherein a fourth transistor provided whose control outputs are connected between the reference voltage terminal and the control output of the third transistor and whose control input is connected to said reference voltage terminal.

6. (Previously presented) The protection circuit according to claim 1, wherein the first transistor (MPI) is a p-channel MOS transistor.

7. (Previously presented) The protection circuit according to claim 5, wherein the second, third and fourth transistor are n-channel MOS transistors.

8. (Previously presented) The protection circuit according to claim 1, wherein the clamping device is a n-channel MOS transistor laid out for ESD protection.

9. (Previously presented) The protection circuit according to claim 1, wherein the clamping device is a parasitic npn transistor.

10. (Previously presented) The protection circuit according to claim 1, wherein the clamping device is a thyristor.

11. (Previously presented) The protection circuit according to claim 1, wherein a diode is connected between the pad and the supply voltage terminal.

12. (Previously presented) An integrated protection circuit for protecting an integrated circuit device, the protection circuit comprising:

a clamping device having a control input and two control outputs, the control outputs including a first control output coupled to a pad and a second control output coupled to a reference voltage terminal;

a first transistor having control outputs connected between the pad and the control input of the clamping device;

a second transistor having control outputs connected between the reference voltage terminal and the control input of the clamping device; and

a time-delay circuit including a resistor and a capacitive device connected in series between a power supply and the control inputs of the first and second transistors, the resistor being connected to the power supply and the capacitive device being connected to the control inputs of the first and second transistors.

13. (Previously presented) The circuit of claim 12, wherein the capacitive device is not directly coupled to the pad.

14. (Previously presented) The circuit of claim 12, wherein the resistor is directly connected to the capacitive device with no intervening circuits.

15. (Previously presented) The circuit of claim 12, further including a diode coupled directly between the power supply and the pad with no intervening circuits, the diode adapted to mitigate current flow from the power supply to the pad.